REMARKS

In view of the preceding amendments and following remarks, reconsideration of the present application is requested. In the Office Action claims 56-65, 72-110, and 112-115 were allowed and claims 1-55, 66-71, and 111 were rejected under 35 U.S.C. §112.

During a telephone conference with the Examiner, an illustrative example of the aim of the current invention was discussed. This same example was included in the (unamended) specification beginning on page 2 at line 17 and ending on page 3 at line 10. As background, applicant believes it may be useful to reiterate it here: "Low cost, high productivity, high accuracy, excellent uniformity and surface quality make wet anisotropic etching a desirable process for deep silicon micromachining. Among some disadvantages of anisotropic etching of (100) orientation silicon is the loss of real estate on the die and wafer surface. As indicated by Figs. 1(A)-(B), the {111) side walls 3 of the etched cavity 1 have about 54 degrees angle to the initial (100) surface of the wafer 2. In order to receive, for example, a square diaphragm 4 with the side one mm, the size of the mask for deep etching to a depth H should be (I+H/$\sqrt{2}$). A silicon wafer of four inches in diameter usually has a thickness of 0.4 mm. Therefore, the mask for 1 mm diaphragms and for deep (almost through) etching should be 1.56 mm. If the width of the frame around the cavity is 0.47 mm, then the total size of the die will be 2.5 x 2.5 mm and a four inch wafer will have about 1000 dies. Theoretically, transition to a six inch wafer should result in doubling the

number of dies (of the same size) because the area is 2.25 times larger than the area of a four inch wafer. However, the thickness of a six 6 inch wafer is larger and usually equals at least 0.6 mm. Therefore, in order to fabricate the same one mm diaphragm, the mask should be 1.85 mm. With the same width of the frame the size of the die will be 2.79 x 2.79 mm instead of 2.5 x 2.5 mm, resulting in a loss of a minimum of 500 dies on each wafer.

Therefore, there is a need for a process of deep micromachining of silicon wafers which will allow about the same real estate for the mask at the surface of the wafer to form the cavities with different depths and the same size at the bottom (diaphragm). This would allow for decrease in the size of the die and its cost."

In the above example, if, as proposed by the applicant, a first etching step other than anisotropic etching were performed prior to the step of deep anisotropic etching, it would be possible to decrease the number of dies lost by moving from the use of a four inch wafer to a six inch wafer. For example, if a first etching step comprising RIE etching to a depth of 0.2 mm were performed on the six inch wafer, i.e. 1/3 of the wafer's thickness of 0.6 mm, it would be possible to fabricate the one mm diaphragm on a six inch wafer using the same mask size used on the four inch wafer; that is, a mask size of 1.56 mm by 1.56 mm, not 1.85 mm by 1.85 mm. With the same width of the frame size it would then be possible to manufacture approximately 2.25 times as many dies on a single six inch wafer than on a single four inch wafer. Analogously, in going from a four inch wafer to an eight inch wafer of thickness 0.8 mm, if the first etch step were

to a depth of 0.4 mm, i.e. 1/2 the initial wafer thickness, then the identical opening size could be used on an eight inch wafer and it would be possible to manufacture four times as many dies on the eight inch wafer as on the four inch wafer. If a process developed for a six wafer were to be carried out on an eight inch wafer using the identical opening size, then the desired depth of the first etch step would be equal to the difference in thickness between six and eight inch wafers; that is, 0.2 mm i.e. 1/4 the initial thickness of the eight inch wafer.

The applicant hopes that the foregoing discussion of material appearing in the Description of the Prior Art serves to clarify the aims of the present invention.

Referring to the Office Action dated July 30, 2003, the Examiner has rejected claims 1-7 and 9-11 under 35 U.S.C. 102 as being anticipated by Laou et al. (5,857,885). Laou discloses a two-step etching process for the fabrication of field emission devices. In column 3 at lines 34-35 Laou discloses "a first etching step to form a shallow cavity, 10, of a depth of 0.2 μm." Also, in column 5 at lines 5-20 Laou discusses "a second etching step"; in particular, at lines 12-14 Laou discloses "The underetching step under the thin film layer, 19, on the shallow cavity, 18, may be 0.2 μm." Thus, the combined etch depth after the first and second etching steps would be 0.4 μm. For field emission devices it is important for the efficacy of the device that the overall (i.e. cumulative) etch depth be very shallow. This is indicated by Laou in column 3 at lines 61-64: "The second etching step is stopped as soon as the tip electrode, 18, is formed. Any further etching will lower the height of the tip electrode 18 and hence increase the tip-to-gate distance." Thus, if the device disclosed by Laou were to

be fabricated using four inch wafers, the overall etch depth would be 1/1000th of the thickness of the wafer. If it were fabricated using six inch wafers, the overall etch depth would be 1/1500th of the thickness of the wafer. The current maximum wafer size is twelve inches with a thickness of about 1.2 mm. If Laou's device were fabricated using twelve inch wafers the overall etch depth would therefore be about 1/3000th of the wafer thickness.

Applicant respectfully points out that the device and method disclosed by Laou is for "shallow" etching, whereas the method for the present invention is, as indicated in the title of the application – "Method for Fabricating Microstructures with Deep Anisotropic Etching of Thick Silicon Wafers" – specifically targeted at "deep" etching. For Laou, "shallow" refers to etch depths on the order of tenths of a micron. For applicant's present invention "deep" is indicated on page 1 at lines 7-8 to mean "comparable to the thickness of the semiconductor wafer"; on page 2 at line 29 "deep" is indicated to mean "almost through". That is, in the context of applicant's invention "deep" refers to etch depths on the order of tenths of millimeters. This is in direct contradistinction to the invention disclosed by Laou. Indeed, if etch depths of this order were used in conjunction with such a device as that disclosed by Laou the resulting device would be decidedly inferior in comparison to field emission devices fabricated using extremely shallow etch depths.

The applicant has amended claim 1 so as to more clearly indicate the desired depths of the two etching steps. As stated at lines 24-27 on page 3 of the Specification, an object of the present invention "is to provide a method of

fabricating cavities with the same size at the bottom (diaphragm) and with an opening mask, which is independent of the initial thickness of the silicon wafer." Step c of claim 1 has been amended to elucidate that the first etch step would be on the order of the difference in thicknesses of standard silicon wafers. As discussed in the example given at the beginning of this response, and appearing on pages 2-3 of the Specification, in adapting a process developed for four inch wafers for use on six inch wafers, the depth of the first etch step on the six inch wafer would be approximately 1/3 of its thickness. In adapting a process developed for four inch wafers to eight inch wafers, the depth of the first etch step on the eight inch wafer would be approximately 1/2 of it thickness. In adapting a process developed for six inch wafers for use on eight inch wafers, the depth of the first etch step on the eight inch wafer would be approximately 1/4 of its thickness. In all these examples the depth of the first etch step is at least 1/4 of the thickness of the wafer, and step c of claim 1 has been amended to include this limitation.

Additionally, step d of claim 1 has been amended to more clearly elucidate that the overall etch depth is to be "almost through" (line 29 on page 2 of the Specification) the silicon wafer. In other words, as indicated in the amended form of step d of claim 1, the depth of this deep anisotropic etch is "comparable to the thickness of the semiconductor wafer", as stated at lines 7-8 on page 1 of the Specification).

Claims 13, 23, 35, and 66 have also been amended to be in independent form including all of the limitations of the base claim and any intervening claims.

Finally, claims 67 and 111 have been amended to correct the spelling of "parylene".

The applicant sincerely hopes that the foregoing is fully responsive to the Examiner's rejections and serves to further elucidate the advantages engendered by the present invention over methods taught in the prior art.

Accordingly, applicant respectfully contends that claims 1-55, 66-71, and 111 are in condition for allowance along with previously allowed claims 56-65, 72-110, and 112-115, and such action is respectfully requested.

If the Examiner is of the opinion that a telephone conference with applicant's attorney will expedite prosecution, such conference is invited.

Respectfully submitted,

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